09/990,474 April 30, 2004 January 30, 2004

Remarks/Arguments:

Amendments

Claim 16, the only dependent claim in the application has been amended. Support for this amendment is found on page 8, line 25, to page 9, line 11. Claims 11 and 20 has been amended to more particularly point out and distinctly claim the subject matter that applicants regard as the invention. It is submitted that no new matter is introduced by these amendments.

Translation

A machine generated English language translation of Kishida, JP 08-022990 ("Kishida) is enclosed.

First Rejection under 35 USC 103

Claims 11, 12, and 16-21 were rejected under 35 USC 103(a) as unpatentable over Arita, U.S. Patent 5,624,864 ("Arita") in view of Kishida, JP 08-022990 ("Kishida). This rejection is respectfully traversed.

Arita discloses a semiconductor device having a capacitor and a manufacturing method thereof. Arita, Title. In Figure 7, an insulating layer **46** and a passivation layer **47** composed of silicon nitride are formed. Arita, column 7, lines 22-30. Charge characteristics of the capacitor **41** were measured after heating for 7 minutes at 380°C after forming passivation layer **47**. Arita, column 8, lines 32-41.

The Office admits that Arita does not show heat-treating the TiN layer before depositing the upper aluminum layer. Office action of 1/30/04, page 3, lines 9-11.

The Office asserts that:

Kishida et al. teach (e.g. Figures 1) to heat treat (i.e. anneal) the TiN layer **5** before directly depositing the Al upper layer **6** using sputtering and heating the circuit board in temperature [range] of 100

09/990,474 April 30, 2004 January 30, 2004

to 400°C to improve step-coverage of an aluminum alloy film in a contact hole. (see Purpose).

Office action of 1/30/04, page 3, lines 11-15.

This assertion is respectively traversed. Kishida does not disclose (1) heat-treating the TiN layer and then (2) depositing the upper metal layer. Kishida discloses a process in which an aluminum alloy film is deposited by sputtering while the skin temperature of the substrate is held at 150 to 250°C. See, Kishida translation, claim 1, lines 6-8; paragraph 8, lines 6-8; and paragraph 15, lines 6-9. These conditions are similar, for example, to the sputtering conditions used by applicants to deposit the upper metal layer. See, specification, page 8, line 25, to page 9, line 11.

This is not the same as applicants' process. Applicants (1) heat-treat the TiN layer and then (2) deposit the upper metal layer. Applicants carry out the heat treatment step before the sputtering step to change the stress in the TiN layer from a compression direction stress to an extensional direction stress. *See*, specification, page 8, lines 19-22. Although the TiN layer will be heated when the upper metal layer is being deposited, the direction of the stress in the TiN layer will not necessarily be changed if the TiN layer is heated while the upper metal layer is being deposited.

Further, neither Arita, Kishida, nor the combination thereof provide any motivation to heat-treat the TiN layer before depositing an upper metal layer. Neither of these references recognizes that compressional direction stress can cause the characteristics of the device to deteriorate. *See*, specification, page 2, line 16, to page 3, line 6. Thus, they provide no motivation to change the stress in the TiN layer by a heat treatment step before depositing the upper metal layer.

The Office has not made the *prima facie* case. Combination of Arita and Kishida in the manner indicated by the Office does not produce applicants' invention. Neither Arita, Kishida, nor the combination thereof disclose or suggest heat-treating the TiN layer before depositing the upper metal layer. Therefore, the rejection of

09/990,474 April 30, 2004 January 30, 2004

claims 11, 12, and 16-21 as unpatentable over Arita in view of Kishida should be withdrawn.

Second Rejection under 35 USC 103

Claims 5, 11, 12, and 16-21 were rejected under 35 USC 103(a) as being unpatentable over Patel, U.S. Patent 5,374,578 ("Patel") in view of Kishida. This rejection is respectfully traversed.

The Office admits that Patel does not show heat-treating the TiN layer before depositing the upper Al layer using sputtering and heating the circuit board in a temperature range of 100 to 400°C. Office action of 1/30/04; page 4, lines 12-14.

As discussed above, Kishida does not disclose heat-treating the TiN layer before depositing the upper metal layer. Further, neither Patel, Kishida nor the combination thereof provide any motivation to heat-treat the TiN layer before depositing an upper metal layer. Neither of these references recognizes that compressional direction stress can cause the characteristics of the device to deteriorate. *See*, specification, page 2, line 16, to page 3, line 6. Thus, they provide no motivation to change the stress in the TiN layer by a heat treatment step before depositing the upper metal layer.

The Office has not made the *prima facie* case. Combination of Patel and Kishida in the manner indicated by the Office does not produce applicants' invention. Neither Patel, Kishida, nor the combination thereof disclose or suggest heat-treating the TiN layer before depositing the upper metal layer. Therefore, the rejection of claims 5, 11, 12, and 16-21 as unpatentable over Patel in view of Kishida should be withdrawn.

Third Rejection under 35 USC 103

Claim 14 was rejected under 35 USC 103(a) as being unpatentable over Arita in view of Kishida, and further in view of Wolf, <u>Silicon Processing for the VLSI Era</u>, Vol. 1, p. 367 (1986) ("Wolf") . This rejection is respectfully traversed.

09/990,474 April 30, 2004 January 30, 2004

As discussed above, neither Arita, Kishida, nor the combination thereof disclose or suggest heat-treating the TiN layer before depositing the upper metal layer. This deficiency is not overcome by Wolf, which was cited for the disclosure of depositing a SiN using PECVD at an RF power of 300 W or less.

The Office has not made the *prima facie* case. Combination of Arita, Kishida, and Wolf in the manner indicated by the Office does not produce applicants' invention. Neither Arita, Kishida, Wolf, nor the combination thereof disclose or suggest heat-treating the TiN layer before depositing the upper metal layer. Therefore, the rejection of claim 14 as unpatentable over Arita in view of Kishida and further in view of Wolf should be withdrawn.

Fourth Rejection under 35 USC 103

Claims 14 was rejected under 35 USC 103(a) as being unpatentable over Patel in view of Kishida, and further in view of Wolf. This rejection is respectfully traversed.

As discussed above, neither Patel, Kishida, nor the combination thereof disclose or suggest heat-treating the TiN layer before depositing the upper metal layer. This deficiency is not overcome by Wolf, which was cited for the disclosure of depositing a SiN using PECVD at an RF power of 300 W or less.

The Office has not made the *prima facie* case. Combination of Patel, Kishida, and Wolf in the manner indicated by the Office does not produce applicants' invention. Neither Patel, Kishida, Wolf, nor the combination thereof disclose or suggest heat-treating the TiN layer before depositing the upper metal layer. Therefore, the rejection of claim 14 as unpatentable over Patel in view of Kishida and further in view of Wolf should be withdrawn.

Conclusion

It is respectfully submitted that the claims are in condition for immediate allowance and a notice to this effect is earnestly solicited. The Examiner is invited to

MTS-2700US1

Application No.: Amendment Dated: Reply to Office Action of: 09/990,474 April 30, 2004 January 30, 2004

phone applicants' attorney if it is believed that a telephonic or personal interview would expedite prosecution of the application.

Respectfully submitted,

Allan Ratner, Reg. No. 19,717 Bruce M. Monroe, Reg. No. 33,602 Attorneys for Applicants

Dated:

April 29, 2004

BMM/bmm/fp

Enclosure:

Translation of Kishida, JP 08-022990

P.O. Box 980 Valley Forge, PA 19482-0980 (610) 407-0700

The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

April 29, 2004

 $\verb|B_{RPFS1\CLIENT\MTS\2700US1\AMEND03.DOC||$